UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,751	04/13/2001	Sergey A. Velichko	303.750US1	4280

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EXAMINER
BARBEE, MANUEL L

ART UNIT	PAPER NUMBER
2857	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	09/834,751	VELICHKO ET AL.
	Examiner	Art Unit	
	MANUEL L. BARBEE	2857	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 August 2008</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>38-43</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>38-43</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
         application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date <u>8/8/08</u>.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 38-40, 42 and 43 are rejected under 35 U.S.C. 103(a) as being

unpatentable over US Patent No. 6,124,725 to Sato (Sato) in view of US Patent No.

6,119,125 to Gloudeman et al. (Gloudeman).

As per claim 38:

        With regard to controlling via a control module concurrent operation of a

        semiconductor test equipment and operation of parametric test instrumentation,

        as shown in claim 29, Sato teaches controlling via a control module (controller

        35) concurrent operation of semiconductor test equipment (wafer chuck 11) and

        parametric test instrumentation (contactor 12, which has a large number of probe

        terminals which are brought into contact with electrode pads of chips formed on a

        wafer, see col. 4, line 10+).

        Sato does not teach that the control module is operable to provide fault-tolerant

        control of the test state via a state oscillator, which is operable to control the state

        of other system modules. Gloudeman teaches a Simple Finite State Machine

        (SFSM) that is an event controller, which changes states based on rules, and

        supports the implementation of a hierarchical state diagram (col. 16, line 41 - col.

17, line 47). The SFSM uses events and inputs to control the state change and synchronize operation with other components (col. 16, lines 51-58; col. 17, lines 39-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor testing, as taught by Sato, to include the SFSM, as taught by Gloudeman, because the operation of different software components together would have been facilitated (Gloudeman, col. 1, lines 19-37).

As per claim 39:

Sato does not teach changing the state of other system modules. Gloudeman teaches a Simple Finite State Machine (SFSM) that is an event controller, which changes states based on rules, and supports the implementation of a hierarchical state diagram (col. 16, line 41 - col. 17, line 47). The SFSM uses events and inputs to control the state change and synchronize operation with other components (col. 16, lines 51-58; col. 17, lines 39-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor testing, as taught by Sato, to include the SFSM, as taught by Gloudeman, because the operation of different software components together would have been facilitated (Gloudeman, col. 1, lines 19-37).

As per claim 40:

Sato does not teach that the state oscillator is controlled in synchronization with other system events by the control module. Gloudeman teaches that the SFSM uses events and inputs to control the state change and synchronize operation

with other components (col. 16, lines 51-58; col. 17, lines 39-47). It would have

been obvious to one of ordinary skill in the art at the time the invention was made

to modify the semiconductor testing, as taught by Sato, to include the SFSM, as

taught by Gloudeman, because the operation of different software components

together would have been facilitated (Gloudeman, col. 1, lines 19-37).

As per claim 42:

With regard to controlling via a control module concurrent operation of a

semiconductor test equipment and operation of parametric test instrumentation,

as shown in claim 29, Sato teaches controlling via a control module (controller

35) concurrent operation of semiconductor test equipment (wafer chuck 11) and

parametric test instrumentation (contactor 12, which has a large number of probe

terminals which are brought into contact with electrode pads of chips formed on a

wafer, see col. 4, line 10+). With regard to providing control of the semiconductor

parametric test equipment via operation of a parametric test equipment module

and providing control of the parametric test instrumentation via operation of a test

instrumentation module, Sato teaches a control module to control the

semiconductor test equipment and parametric test instrumentation (col. 4, lines

10+).

Sato does not teach that the control module is operable to provide fault-tolerant

control of the test state via a state oscillator, which is operable to control the state

of other system modules. Gloudeman teaches a Simple Finite State Machine

(SFSM) that is an event controller, which changes states based on rules, and

supports the implementation of a hierarchical state diagram (col. 16, line 41 - col.

17, line 47). The SFSM uses events and inputs to control the state change and

synchronize operation with other components (col. 16, lines 51-58; col. 17, lines

39-47). It would have been obvious to one of ordinary skill in the art at the time

the invention was made to modify the semiconductor testing, as taught by Sato,

to include the SFSM, as taught by Gloudeman, because the operation of different

software components together would have been facilitated (Gloudeman, col. 1,

lines 19-37).

As per claim 43:

With regard to controlling via a control module concurrent operation of a

semiconductor test equipment and operation of parametric test instrumentation,

as shown in claim 29, Sato teaches controlling via a control module (controller

35) concurrent operation of semiconductor test equipment (wafer chuck 11) and

parametric test instrumentation (contactor 12, which has a large number of probe

terminals which are brought into contact with electrode pads of chips formed on a

wafer, see col. 4, line 10+). With regard to providing control of the semiconductor

parametric test equipment via operation of a parametric test equipment module

and providing control of the parametric test instrumentation via operation of a test

instrumentation module, Sato teaches a control module to control the

semiconductor test equipment and parametric test instrumentation (col. 4, lines

10+).

Sato does not teach that the control module is operable to provide fault-tolerant control of the test state via a state oscillator, which is operable to control the state of other system modules. Gloudeman teaches a Simple Finite State Machine (SFSM) that is an event controller, which changes states based on rules, and supports the implementation of a hierarchical state diagram (col. 16, line 41 - col. 17, line 47). The SFSM uses events and inputs to control the state change and synchronize operation with other components (col. 16, lines 51-58; col. 17, lines 39-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor testing, as taught by Sato, to include the SFSM, as taught by Gloudeman, because the operation of different software components together would have been facilitated (Gloudeman, col. 1, lines 19-37).

3.   Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato in view of Gloudeman as applied to claim 38 above, and further in view of US Patent No. 5,206,582 to Ekstedt et al. (Ekstedt).

Sato and Gloudeman teach all the limitations of claim 38 upon which claim 41 depends. Sato and Gloudeman do not teach an abort superstate, a pause superstate and a lot run superstate. Ekstedt teaches exiting the testing loop when a defective device is found, pausing for user input and the normal testing routine (col. 11, lines 4-35; col. 10, lines 32-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor testing combination, as taught by Sato and Gloudeman, to include

the states taught by Ekstedt, because then known system states would have

been handled modularly.

Response to Arguments

4.   Applicant's arguments filed 8 August 2008 have been fully considered but they

are not persuasive.

Applicant states that Sato does not teach concurrent operation of semiconductor

test equipment and parametric test instrumentation, as is recited in the pending claims,

but instead teaches only sequential operation of various semiconductor test equipment.

However, Sato teaches controlling via a control module (controller 35) concurrent

operation of semiconductor test equipment (wafer chuck 11) and parametric test

instrumentation (contactor 12, which has a large number of probe terminals which are

brought into contact with electrode pads of chips formed on a wafer, see col. 4, line

10+). Applicant argues that Sato teaches throughout that only after the contactor is in

contact with the wafer under test does Sato's switcher switch sequentially between an

electric characteristic test mechanism and a reliability test mechanism. Applicant further

states that Sato's contactor is defined in the pending application and claims as

semiconductor test equipment. However, claim 38, for example recites limitations for

"controlling via a control module concurrent operation of semiconductor test equipment

and operation of parametric test instrumentation." No further definition is given for

"semiconductor test equipment" and "parametric test instrumentation" in the claims.

Applicant states that Gloudeman fails to teach a state oscillator module that

controls the state of other modules. However, the SFSM uses events and inputs to

control the state change and synchronize operation with other components (col. 16,

lines 51-58; col. 17, lines 39-47).

Applicant argues that Gloudeman and Sato are from different fields and provide

no motivation combine to address the present problem. However the ability to control

two or more software components is a common problem. Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify

the semiconductor testing, as taught by Sato, to include the SFSM, as taught by

Gloudeman, because the operation of different software components together would

have been facilitated (Gloudeman, col. 1, lines 19-37).

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MANUEL L. BARBEE whose telephone number is

(571)272-2212. The examiner can normally be reached on Monday-Friday from 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Manuel L. Barbee/
Primary Examiner, Art Unit 2857

mlb
November 22, 2008